REMARKS

In response to the Office action of April 26, 2010, please enter the amendments set forth above and consider the following remarks. By this response, Applicants amend claims 7 and 10. No new matter has been added. Following entry of these papers, claims 1-2, 4-5, 7, and 9-21 will remain pending.

In the Office Action, the Examiner (i) rejected claims 7 and 10 under 35 U.S.C. 101 as directed to non statutory subject matter; and (ii) rejected claim 1-2, 4-5, 7, and 9-21 as being unpatentable over U.S. Patent 5,587,962 (Hashimoto) in view of U.S. Patent 5,973,664 (Badger) in further view of U.S. Patent 6,904,473 (Bloxham). Applicants respectfully traverse. In the interest of efficiently furthering prosecution, Applicants have amended claims 7 and 10. Applicants respectfully submit that the claims as amended are allowable over the cited art for at least the reasons set forth below. Reconsideration is requested.

I. The Examiner rejected claims 7 and 10 as directed to non-statutory subject matter. Applicants have amended claims 7 and 10 to depend from claims 2 and 5, respectively, and to clarify the recitations of the claims. Applicants respectfully submit that claims 7 and 10 as amended recite statutory subject matter, and request that the rejection under 35 U.S.C. 101 be withdrawn.

II. The rejected claim 1-2, 4-5, 7, and 9-21 as being unpatentable over U.S. Patent 5,587,962 (Hashimoto) in view of U.S. Patent 5,973,664 (Badger) in further view of U.S. Patent 6,904,473 (Bloxham). III. The Examiner rejected claims 1, 7, 15, and 35 under 35 U.S.C. 103 as being unpatentable over Lin in view of U.S. Patent 5,175,747 (Murakami).

Claim 1 as recites “operating the driving circuit alternately in a first mode wherein the address sequencer generates addresses for the video data in the memory by combining line pointers that are read out by a line counter from a block of line pointers in address table register means with the output of a pixel counter using an adder, and in

a second mode wherein a block of line pointers from the full table of line pointers that is stored in said memory is downloaded into said address table register means". One potential implementation of the above recitations of claim 1 may be described in Figs. 1 and 2 and in page 4 line 13 through page 5 line 24 of the present application. In one potential implementation, a first mode provides a portion of video data to a driving circuit, and a second mode loads a portion of remaining address data into a table in preparation for reading an additional portion of video data to the driving circuit.

As discussed by the Examiner on page 4, while Hashimoto discusses a driving circuit with two operating modes, the two modes are completely different than the two modes recited above by claim 1.

On page 5 of the present Office action, the Examiner asserts that the two modes detailed by the above recitation of claim 1 are found separately in Badger and Bloxham. The Examiner further states that "the memory address is generated from combining Y_counter and X_counter, associated with the line pointer and pixel counter. The steps 806 and 810 involve additions, which means that a[n] adder, or its equivalence, is present". In Berger, however, the values being combined with an adder are not line pointers and pixel counters, as recited by claim 1. In Berger element 806, Mem_pointer is incremented by a pixel size amount, Screen_pointer is incremented by an X_increment amount, and X_counter is decreased by 1 (See Berger Col. 8 lines 34-39). In Berger element 810, Screen_Pointer is incremented by Y_Increment, and a value equal to X_Increment times Logical_Width is subtracted from Screen_Pointer. Finally in 810, Y_counter is decreased by 1 (See Berger Col. 8 lines 40-60). None of these recitations in Berger element 806 or 810, or anywhere in Berger, discloses the recitation of claim 1 above.

Similarly, while Bloxham describes reading data stored consecutively into a memory, Bloxham does not teach or suggest ""operating the driving circuit alternately in a first mode wherein the address sequencer generates addresses for the video data in the memory by combining line pointers that are read out by a line counter from a block of line pointers in address table register means with the output of a pixel counter using

an adder, and in a second mode wherein a block of line pointers from the full table of line pointers that is stored in said memory is downloaded into said address table register means".

Further, The Examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness (MPEP 2142). To find a claim unpatentable due to obviousness under § 103(a), an examiner must engage in a factual inquiry involving:

> (A) Ascertaining the scope and content of the prior art;
> (B) Ascertaining the differences between the claimed invention and the prior art; and
> (C) Resolving the level of ordinary skill in the pertinent art.
> (MPEP 2141 and *Graham v. John Deere Co.*, 383 U.S. 1)

Additionally, "rejections under 35 U.S.C. 103 "cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" (MPEP 2143, citing the Federal Circuit in *In re Kahn*, 441 F.3d 977, 988, 78 USPTQ2d 1329, 1336 (Fed. Cir. 2006)).

As described in the present application, for example in the first paragraphs of page 3, the above discussed recitations of claim 1 function to reduce costs by decreasing the required size of a memory component. Applicants respectfully submit that the Examiner has not disclosed an acceptable basis to support a legal conclusion of obviousness both because the references do not teach every element of the independent claims, and because there is not acceptable rational present supported by the references to sustain a combination of the references as presented by the Examiner.

As such, Applicants respectfully submit that claim 1 is not obvious given the cited art, and the rejection of claim 1 under 35 U.S.C. 103 should be withdrawn.

Additionally, since claims 2 and 9 include recitations similar to those of claim 1 discussed above, and claims 4-5, 7, and 10-21 depend from claims 1, 2, and 9, Applicants respectfully submit that the rejection should be withdrawn, and the claims deemed allowable over the cited art.

Conclusory Remarks

In view of the above, it is respectfully submitted that claims 1-2, 4-5, 7, and 9-21 as amended are allowable over the cited art and are now in condition for formal allowance, and early and favorable action to that end is respectfully requested.

The Examiner is encouraged to call Applicants' attorney at the number below if doing so will in any way advance prosecution of this application.

The Commissioner is hereby authorized to charge any fees which may be required, or credit in the overpayment, to Deposit Account No. **07-1896** referencing Attorney Docket No. **348162-982280**.

Respectfully submitted,

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